CLAIMS:

1. A method of designing an integrated circuit having a plurality of logic paths, comprising:

designing the integrated circuit in accordance with timing constraint data;

identifying any logic paths in said plurality of logic paths that have a timing characteristic within a threshold to define a first set of logic paths, where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths; and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths.

2. The method of claim 1, wherein said selectively optimizing comprises:

power optimizing only said second set of logic paths.

3. The method of claim 2, wherein said power optimizing comprises:

synthesizing said second set of logic paths;

mapping said second set of logic paths onto primitive components of a target device;

placing said second set of logic paths with respect to said target device; and

routing connections of said second set of logic paths.

4. The method of claim 1, wherein said selectively optimizing comprises:

power optimizing said first set of logic paths and said second set of logic paths; and

determining whether said timing characteristic of any logic paths in said first set of logic paths has been

modified beyond a threshold to define a third set of logic paths.

5. The method of claim 4, wherein said power optimizing comprises:

synthesizing said first set of logic paths and said second set of logic paths;

mapping said first set of logic paths and said second set of logic paths onto primitive components of a target device;

placing said first set of logic paths and said second set of logic paths with respect to said target device; and

routing connections of said first set of logic paths and said second set of logic paths.

6. The method of claim 4, further comprising at least one of:

rejecting a power optimization for each logic path in said third set of logic paths; and

reporting a timing constraint violation for each logic path in said third set of logic paths.

7. The method of claim 1, further comprising:

identifying logic paths in at least one of said first set of logic paths and said second set of logic paths that violate said timing constraint data to define a third set of logic paths.

8. The method of claim 7, further comprising at least one of:

rejecting a power optimization for each logic path in said third set of logic paths; and

reporting a timing constraint violation for each logic path in said third set of logic paths.

9. The method of claim 1, wherein said threshold is defined by a percentage of a parameter in said timing constraint data.

10. The method of claim 1, wherein said threshold is defined by an absolute value with respect to a parameter of said timing constraint data.

11. A computer readable medium having stored thereon instructions that, when executed by a processor, cause the processor to perform a method of designing an integrated circuit having a plurality of logic paths, comprising:

designing the integrated circuit in accordance with timing constraint data;

identifying any logic paths in said plurality of logic paths that have a timing characteristic within a threshold to define a first set of logic paths, where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths; and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths.

12. The computer readable medium of claim 11, wherein said selectively optimizing comprises:

power optimizing only said second set of logic paths.

13. The computer readable medium of claim 11, wherein said selectively optimizing comprises:

power optimizing said first set of logic paths and said second set of logic paths;

determining whether said timing characteristic of any logic paths in said first set of logic paths has been modified beyond a threshold to define a third set of logic paths; and

at least one of:

rejecting a power optimization for each logic path in said third set of logic paths; and

reporting a timing constraint violation for each logic path in said third set of logic paths.

14. An apparatus for designing an integrated circuit having a plurality of logic paths, comprising:

means for designing the integrated circuit in accordance with timing constraint data;

means for identifying any logic paths in said plurality of logic paths that have a timing characteristic within a threshold to define a first set of logic paths, where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths; and

means for selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths.

15. The apparatus of claim 14, wherein said means for selectively optimizing comprises means for power optimizing only said second set of logic paths.

16. The apparatus of claim 14, wherein said means for selectively optimizing comprises:

means for power optimizing said first set of logic paths and said second set of logic paths;

means for determining whether said timing characteristic of any logic paths in said first set of logic paths has been modified beyond a threshold to define a third set of logic paths; and

at least one of:

means for rejecting a power optimization for each logic path in said third set of logic paths; and

means for reporting a timing constraint violation for each logic path in said third set of logic paths.

17. A method of designing an integrated circuit, comprising:

designing the integrated circuit in accordance with timing constraint data;

identifying timing critical logic circuitry; and

selectively optimizing the integrated circuit to reduce power consumption in response to said timing critical circuitry.

18. The method of claim 17, wherein said selectively optimizing comprises:

power optimizing logic circuitry within said integrated circuit other than said timing critical logic circuitry.

19. The method of claim 17, wherein said selectively optimizing comprises:

power optimizing said integrated circuit;

determining whether a timing characteristic of said timing critical circuitry has been modified beyond a threshold; and

responsive to said timing characteristic being modified beyond a threshold, at least one of:

rejecting a power optimization of said timing critical circuitry; and

reporting a timing violation.

20. The method of claim 17, wherein said timing critical circuitry is defined with respect to at least one timing constraint parameter.